I Introduction

I.I General

The following is taken from LEON user's manuals of the XST edition:

The LEON VHDL model implements a 32-bit processor conforming to the IEEE-1754 (SPARC V8) architecture. It is designed for embedded applications with the following features on-chip: separate instruction and data caches, hardware multiplier and divider, interrupt controller, debug support unit with trace buffer, two 24-bit timers, two UARTs, power-down function, watchdog, 16-bit I/O port, flexible memory controller, ethernet MAC and PCI interface.

I.II Goals and Motivation

- Run the entire flow from RTL to place and route design using the free XST Release 7.1i.
- Supply and document the assorted results of the follow.

II Summary of Results

II.I Gate Count

Total equivalent gate count for design: 1,433,586 as reported in test_map.mrp.

II.II Number Flip Flops

Slice Flip Flops driven by IOB = 1153
Slice Flip Flops = 3233

II.III RAMs

Number used for Dual Port RAMs: 1,152
Number of Block RAMs: 19

II.IV Timing

Constraint	Requested	Actual	Logic Levels
TS_clk = PERIOD TIMEGRP "clk" 40 ns HIGH 50%	40.000ns	39.351ns	10
OFFSET = IN 7 ns BEFORE COMP "clk"	7.000ns	4.396ns	0
OFFSET = OUT 12 ns AFTER COMP "clk"	12.000ns	11.528ns	1

II.V XILINX Part Number

Target Device : xc3s1500l
Target Package : fg676
Target Speed   : -4
Mapper Version : spartan3 --