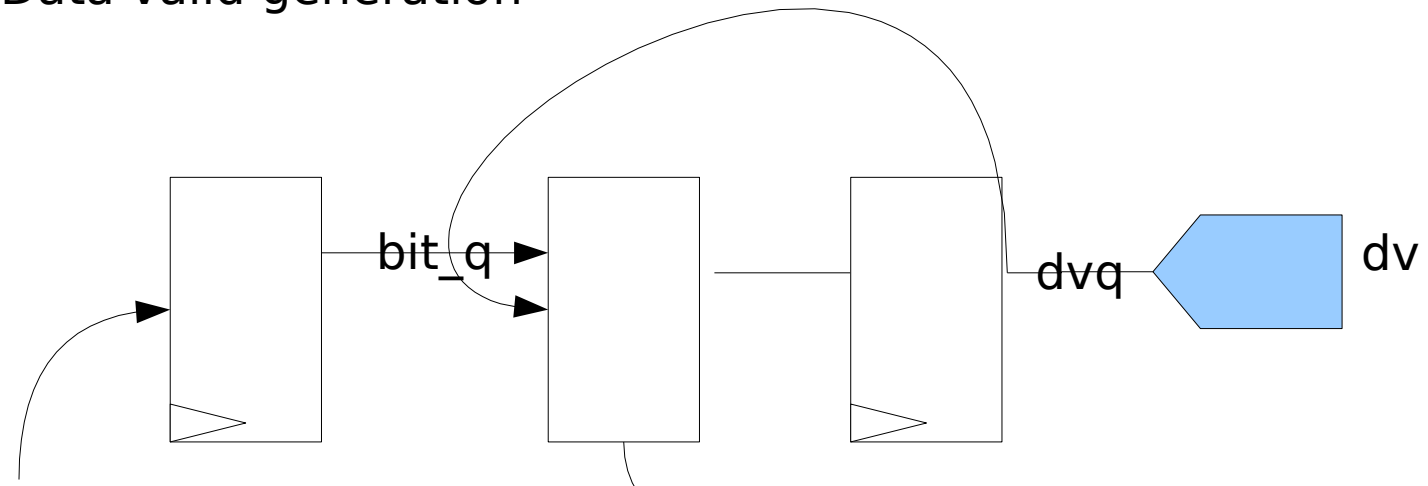
Data valid generation




```
assign {erri, bit_i}=
!bit_eq                    ? 3'b0_00 :
//
(bit_q == 2'd3 && shf_q == 4'h0) ? 3'b0_00 :
(bit_q == 2'd3 && shf_q == 4'h1) ? 3'b0_01 :
(bit_q == 2'd3 && shf_q == 4'h2) ? 3'b1_00 :
(bit_q == 2'd3 && shf_q == 4'h3) ? 3'b0_10 :
(bit_q == 2'd3 && shf_q == 4'h4) ? 3'b1_00 :
(bit_q == 2'd3 && shf_q == 4'h5) ? 3'b1_00 :
//(bit_q == 2'd3 && shf_q == 4'h6) ? 3'b0_11 ://meta-stable
(bit_q == 2'd3 && shf_q == 4'h6) ? 3'b1_00 ://meta-stable
(bit_q == 2'd3 && shf_q == 4'h7) ? 3'b0_11 :
(bit_q == 2'd3 && shf_q == 4'h8) ? 3'b0_11 :
//(bit_q == 2'd3 && shf_q == 4'h9) ? 3'b0_11 ://meta-stable
(bit_q == 2'd3 && shf_q == 4'h9) ? 3'b1_00 ://meta-stable
(bit_q == 2'd3 && shf_q == 4'ha) ? 3'b1_00 :
(bit_q == 2'd3 && shf_q == 4'hb) ? 3'b1_00 :
(bit_q == 2'd3 && shf_q == 4'hc) ? 3'b0_10 :
(bit_q == 2'd3 && shf_q == 4'hd) ? 3'b1_00 :
(bit_q == 2'd3 && shf_q == 4'he) ? 3'b0_01 :
(bit_q == 2'd3 && shf_q == 4'hf) ? 3'b0_00 :
{1'b0, bit_i1};
```

bit_q == 3'd3 && !dvq

bit_q is pahse correct counter

If TX and RX use a synchronous clock, the count would go 0,1,2,3,0...